REMARKS

Claims 2-30 are pending in the present application. Claims 9 and 15, 18, 20-28, and 30 have been rejected, with all other claims having been indicated as being allowable. Claims 9, 16 and 21 are amended herein. Consideration of these remarks and allowance of the claims is respectfully requested.

Applicant wishes to thank the Examiner for allowing claims 2-8 and 10-14 and indicating the allowable subject matter of claims 16, 17, 19 and 29. In view of this indication, Applicant has amended claim 16 to be in independent form. Accordingly, claims 16, 17 and 19 should now be allowable.

Claims 9 and 21 were objected to based on informalities. Each of these claims has been amended as suggested by the Examiner. Neither of these amendments narrows the scope of any claim.

Claims 9, 15, 18, 20-28 and 30 have been rejected under 35 U.S.C. 102(b) as being anticipated by Hanson, *et al.* (U.S. Patent No. 6,181,165) and claim 28 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Hanson, *et al.* Applicant respectfully traverses this rejection.

Claim 9 specifically recites "an input node to receive an input signal, the input signal varying between the first voltage level and the second voltage level; . . . a second n-channel transistor having . . . a second source/drain region coupled to the second voltage level reference node and a gate coupled to a first enable signal node; [and] a second p-channel transistor having . . . a second source/drain region coupled to the third reference node and a gate coupled to a second enable signal node." Applicant respectfully submits that the reference by Hanson, *et al.* does not teach or suggest the limitations of claim 9.

In the rejection, the Examiner analyzes Hanson, *et al.* by stating that the first voltage

level is about 1 V (based upon column 2, lines 18-20), the second voltage level is ground, and the third voltage level is VDD. Applicant respectfully submits that this analysis is based upon a misreading of the reference.

Figure 1 of Hanson, *et al.* illustrates "a simplified prior art inverting tri-state buffer circuit 100." Col. 1., line 23. There is no indication that the circuit of Figure 1 can provide any level shifting capabilities as required by claim 9. As noted by the Examiner, the reference does, however, discuss the capability of using this circuit as a "reduced voltage input/reduced voltage output tri-state buffer circuit." Col. 2, lines 3-4. To facilitate discussion, the first two paragraphs of column 2 are repeated here. According to the Office Action, these paragraphs are being relied upon by the Examiner to find anticipation of the pending claims.

> Another disadvantage of the configuration shown in FIG. 1 relates to the fact that inverting tri-state buffer 100 is generally incapable of functioning as a reduced voltage input/reduced voltage output tri-state buffer circuit. Reduced voltage input refers to input voltages that are lower than the full V_{DD} supplied to the chip. In some cases, the reduced voltage may be low enough (e.g., 1V) that it approaches the threshold voltage of the transistors (typically at 0.7 V or so). Likewise, reduced voltage output refers to output voltages that are lower than the full V_{DD} supplied to the chip. Since reduced voltage signals (i.e., signals whose amplitude is within the reduced voltage range) are useful in reducing circuit power consumption, the inability of inverting tri-state buffer 100 to function as a reduced voltage buffer represents a serious shortcoming.
>
> To appreciate the problems encountered in buffering reduced voltage signals, consider the situation wherein the input of inverting tri-state buffer 100 is logically high but is represented by a reduced voltage signal (e.g., around 1 V). In this case, not only does n-FET 106 conduct as expected but p-FET 104 may also be softly on, causing leakage current to traverse p-FET 104 (from V_{DD} through p-FET 102). The presence of the leakage current degrades the signal on the output of the buffer circuit (and/or greatly increasing power consumption).

Col. 2, lines 1-25.

In this section, Hanson, *et al.* states that buffer 100 is "generally incapable of functioning

as a reduced voltage input/reduced voltage output tri-state buffer circuit."[1] In other words, in this discussion both the input and the output are "reduced voltage." The reference simply never teaches a case where the input carries a reduced voltage and the output carries a full voltage (V_{DD}). Therefore, it is respectfully submitted that the Hanson, *et al.* does not teach or suggest the limitations of claim 9.

Claims 15 and 18 depend from claim 9 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding further limitations.

Claim 20 specifically recites "a level-shifting section responsive to an input logic signal, the input logic signal varying between a first voltage level and a second voltage level, the level-shifting section providing an output logic signal at an output terminal thereof, the output logic signal varying between the first voltage level and a third voltage level, the third voltage level being different than the second voltage level." Applicant respectfully submits that the references of record do not teach or suggest the limitations of claim 20.

As discussed above, Hanson, *et al.* does not teach an input logic signal varying between a first voltage level and a second voltage level and an output logic signal varying between the first voltage level and a third voltage level. While Hanson, *et al.* may teach a first situation where both the input and output vary between ground and V_{DD} and a second situation where both the input and output vary between a reduced voltage and ground, Hanson, *et al.* never teaches or suggests a circuit where the input logic signal and the output logic signal vary between different voltage levels. Therefore, it is respectfully submitted that claim 20 is allowable over the references of record.

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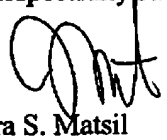
[1] For the purposes of this discussion, Applicant will assume that Hanson teaches a reduced voltage input/reduced voltage output tri-state buffer circuit. Applicant reserves the right to argue this point later.

Claims 21-30 depend from claim 20 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding further limitations.

In view of the above, Applicant respectfully submits that the formal issues have been resolved. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's agent at the below listed telephone number and address. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,



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